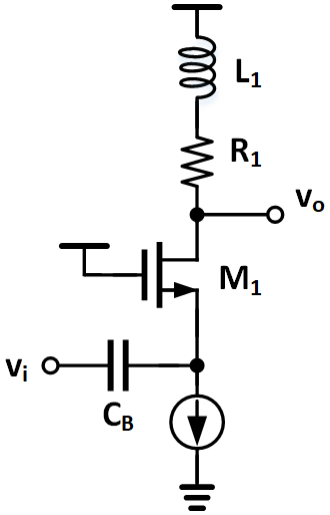
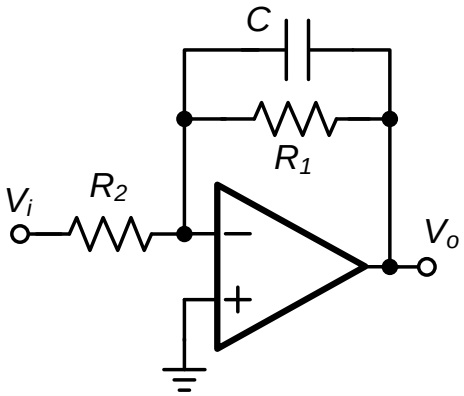
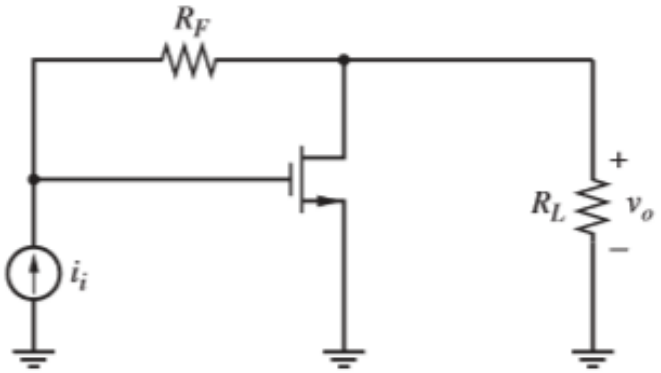
1. [15 pts] The circuit under analysis is as shown as in the following figure. M_1 is not ideal. That is, there exist C_{gs}, C_{gd}, and transistor output resistance r_o. Let C_B be an ideal dc block at the input. Assume $\omega L_1/R_1 > 3$.
   a. What is the frequency when the maximum voltage gain occurs?
   b. Formulate and find out the value of the maximum voltage gain, v_o/v_i.



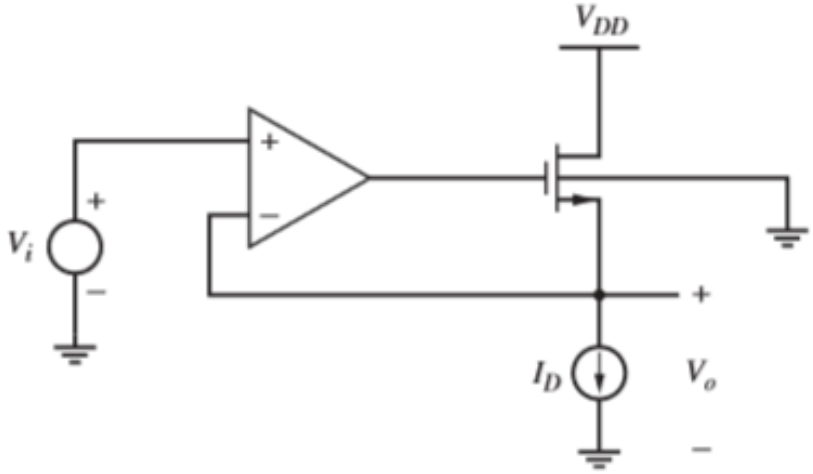
2. [10 pts] Assume the operational amplifier is ideal. Design the circuit such that the input impedance is 500 Ω, voltage gain is 20 dB, and the frequency of unity gain is at 2000 rad/sec.



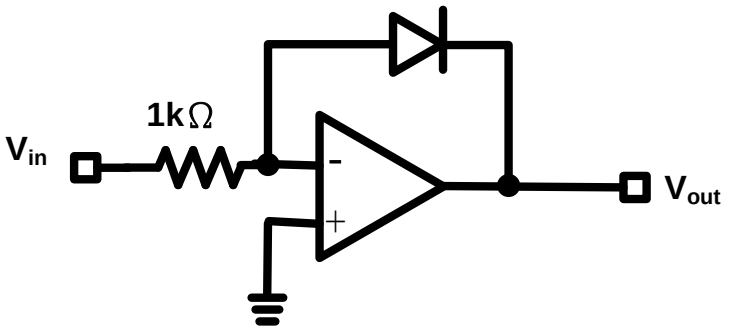
3. [10 pts] Consider an ac schematic of a local shunt-shunt feedback circuit shown below. For the MOS transistor, I_D = 0.5mA, W/L = 100, k' = 200 μA/V^2, and $r_o = \infty$. If R_F = 200kΩ, and R_L = 50kΩ. Please calculate input resistance, out resistance, loop transmission, and close-loop gain.



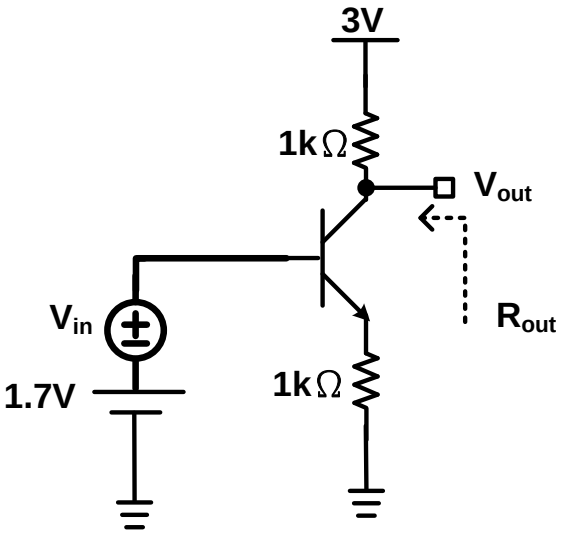
4. [15 pts] A voltage-follower feedback circuit is shown below. For the MOS transistor, I_D = 0.5 mA , k' = 180 μA/V^2, $r_o = \infty$, W/L = 100, $|\varphi_f|$ = 0.3 V, and γ = 0.3 V$^{1/2}$. For the op amp, assume that the input resistance R_i = 1 MΩ, the output resistance R_o = 10 kΩ, and the voltage gain a_v = 1,000. Please calculate input resistance, output resistance, loop transmission, and closed-loop gain:



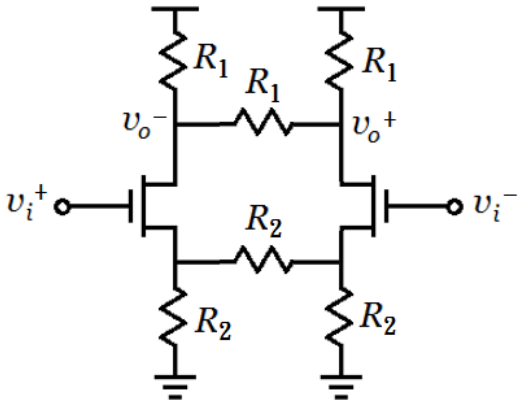
5. [15 pts] In the schematic shown below, assume the operational amplifier is ideal. The diode has a I-V curve of: $I_D = I_s\left(e^{\frac{V_D}{V_T}} - 1\right)$, with $V_T = 25mV$ and $I_s = 1nA$. The diode has a reverse breakdown voltage of 10 V.
   a. Please plot the relationship between V_{out} and V_{in}. You will need to provide your calculation process.
   b. What is the output voltage V_{out} when $V_{in} = 1V$.
   c. Can you identify the range of V_{in} that the diode will be damaged?



6. [10 pts] For the amplifier shown below, V_{in} is assumed to be a small signal source. The BJT has $\beta = 100$, and $V_A = 20V$. Ignore all parasitic capacitance, and assume $25mV$ thermal voltage.
   a. What is the small signal gain (V_{out}/V_{in})?
   b. What is the output resistance (R_{out})?



7. [10 pts] Consider the differential amplifier shown below. Assume that all the transistors are biased in the saturation region. Neglect the body effect and the channel-length modulation effect. Let $g_m = 1$ mA/V, $R_1 = 20\,\text{k}\Omega$, $R_2 = 1\,\text{k}\Omega$. Find the common-mode-rejection ratio CMRR.



8. [15 pts] Consider the differential amplifier shown below. Assume that all the transistors are biased in the saturation region. Neglect the body effect. Let $g_m = 1$ mA/V, $r_o = 20\,\text{k}\Omega$ for all the transistors.
   a. Find the output resistance of the amplifier.
   b. Find the small-signal gain of the amplifier $v_o/(v_i^+ - v_i^-)$.