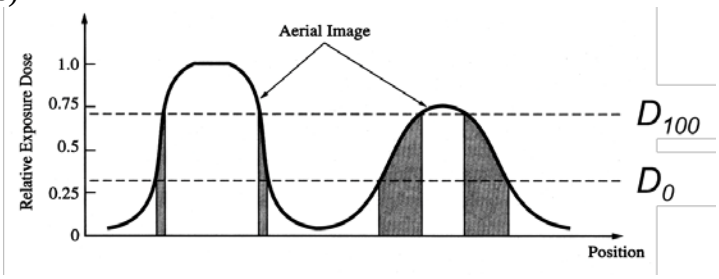
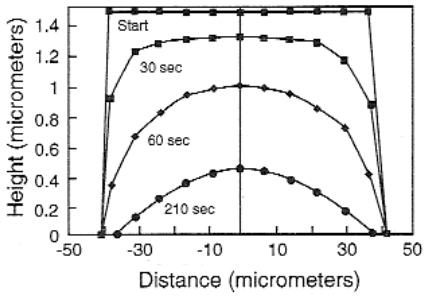
1. For the two aerial images shown in figure, estimate the modulation transfer functions (MTF) and the critical modulation transfer functions (CMTF). Which one can result in more vertical PR sidewall? (**5 pts**)



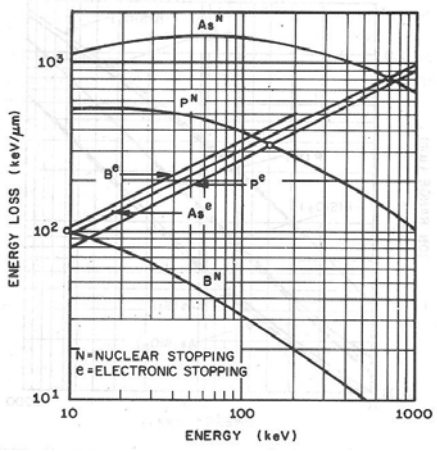
2. Does post-exposure baking reduce standing wave effect in both i-line PR and DUV PR? Why? (**5 pts**)

3. Cu-interconnect has replaced Al-based interconnect since 180 nm technology generation. (a) Explain the reason from the points of resistance, capacitance, electro-migration, and stress migration. (b) Cu is deposited by electro-chemical plating, explain the advantages of pulse mode ECD with respect to DC mode ECD. (c) Explain the mechanism of bottom-up filling. (**10 pts**)

4. Explain the reason for the topography evolution during oxide CMP shown in figure. (**5 pts**)



5. According to the figure of stopping power, if phosphorus ions are implanted into Si at 200 keV, will the Si surface or deep be damaged more serious? Why? (**5 pts**)



6. Explain the mechanism of transient enhanced diffusion. Will the TED be more serious at 700 °C or 100 °C? (**5 pts**)

7. (a) Please describe the advantages and disadvantages of the chemical vapor deposition (CVD) and physical vapor deposition (PVD). (**5 pts**)
   (b) What kinds of CVD and PVD schemes are often applied for the metal depositions of the nm-scale devices? (**5 pts**)

8. (a) Please compare the mechanisms of the reactive ion etching (RIE) and plasma etching (PE). (**5 pts**)
   (b) Please describe the techniques of the high-density-plasma (HDP) etching. (**5 pts**)

9. (a) Please explain the mechanism of the atomic-layer-deposition (ALD). (**5 pts**)
   (b) Please describe the depositions of the high-K gate dielectrics using the ALD technique. (**5 pts**)

10. Please detail the advantages and penalties due to Fluorine incorporation in front-end process and the solutions to fix the problems
    (a) The advantages and penalties due to Fluorine incorporation in CMOS devices (nMOS and pMOS) in terms of performance, reliability, and scaling (**6 pts**)
    (b) The solutions to solve the problems due to Fluorine incorporation (**6 pts**)

11. The gate stack with poly-Si gate/SiO_2 has maintained its dominant role in CMOS device fabrication for more than 50 years (a) what are the advantages specific to the poly-Si gate/SiO_2 (**6 pts**) (b) what are the limitations of poly-Si gate for CMOS scaling below 100 nm regime? (**5 pts**)

12. High-K gate stack for sub-100 nm Si CMOS technologies
    (a) Identify the major challenges to high-K gate stack for Si CMOS manufacturing and explain the underlying mechanisms (**4 pts**)
    (b) Propose the solutions of high-K gate stack for manufacturing (**4 pts**)
    (c) Make a comparison and identify the differences between the planar bulk Si and FD UTB (fully depleted ultra-thin body) or multi-gate FET (FinFET) in high-K gate stack technologies (**4 pts**)