1. [16%] Parallel multiplier is demanded in many applications to reach real-time performance.
(a) [6%] Explain how Booth encoding is exploited to reduce the number of partial products. You may derive a coding table and explain how partial products can be reduced by half.
(b) [6%] Explain why 1-bit full-adder can be used as the basic element of the parallel multiplier.
(c) [4%] How do you modify the 1-bit full-adder to allow signed multiplication in partial product generation?

2. [18%] The following equation, $Z=\sum A_i*W_i$, i=1..N, is often found in signal and data analysis applications.
(a) [6%] Modify the parallel multiplier so that A*B+C is allowed, where only one extra full-adder layer is needed.
(b) [6%] Assume that A_i and W_i are stored in SRAM, how do you design a datapath so that the Z can be completed in N cycles. Draw the block diagram of your design and explain how it works.
(c) [6%] If multiple datapaths are allowed, how do you modify the above design in 2(b) so that Z can be completed in N/2 cycles or less? Note that you should take the memory bandwidth into account.

3. [16%] <u>Explain the following glossaries definitely and briefly.</u>

(a) [4%] Design a high-skew (with DC logic threshold voltage higer than Vdd/2) Inverter and explain its usage in logic design
(b) [4%] What is the usage of the feedback PMOS in a domino circuit shown in Fig.1(a)?
(c) [8%] There are layers of contact, P/N-diffusion, metal and poly drawn for 2-input NAND in Fig.1 (b): (i) Which layout is better for delay time? Why? (ii) What are the concerns to put the latest arriving signal (input B) to the transistor near the output of the gate

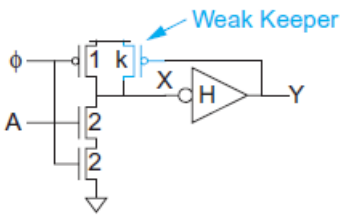
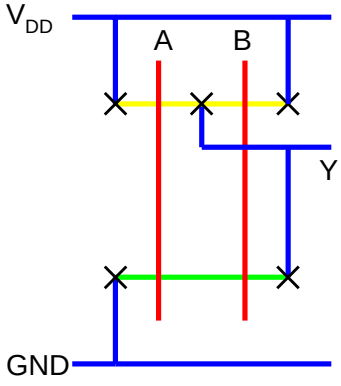


Fig.1(a)



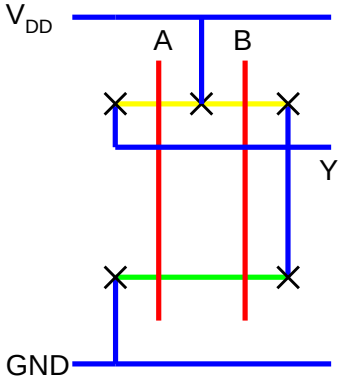


Fig.1 (b)

4. [16%] Logic Design:

(a) [8%] Draw the transistor-level CMOS circuit diagrams for function $\overline{A + B(C + D)}$ (try to use minimum number of transistor). Size and mark the W/L ratio of each transistor in the gate such that the circuit has similar delay of a typical unit size inverter. **You must explain your sizing principle**. A typical unit size inverter by using 45 nm CMOS process has W/L=45/45 (in nm) for NMOS transistors and 90/45 (in nm) for PMOS transistors

(b) [8%] Clock Gating of flip-flop is a method to reduce power consumption of synchronous digital IC. Fig.2 lists two methods of clock gating scheme. Please dercribe the behavior and discuss the advatnges and disadvantage of these two methods.

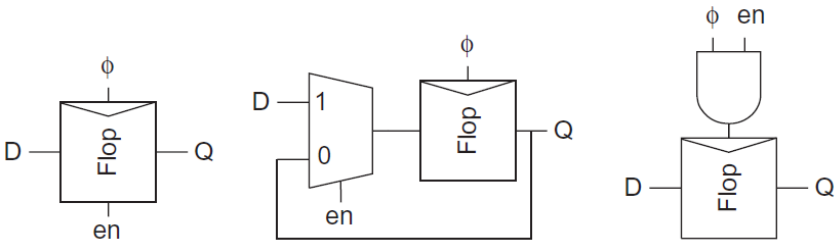
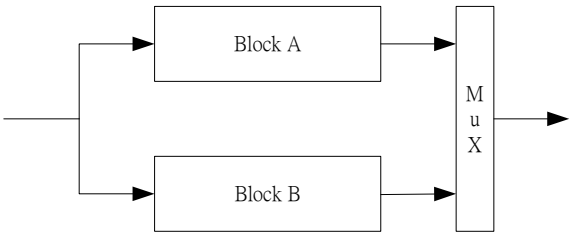


Fig.2

5. [22%] Low Power Design:

As shown in the figure, each block (A or B) contains two parts: clock tree, and logic operation. The following table lists the capacitance, C_{clock} and C_{logic}, as well as other information you need to know for power calculation ($\mathbf{Power} = \sum \alpha C V^2 f$). Assume operating frequency is kept the same for all cases



	clock part			logic part		
Block A	**alpha**	**c**	**V**	**alpha**	**C**	**V**
Original	1	1	1	0.25	2	1
Pipeline	1	1.1	0.7	0.25	2.5	0.7
Parallel	1	1.5	0.6	0.25	3	0.6
pipeline+clock gating	0.1	1.1	0.7	0.25	2.6	0.7
parallel+clock gating	0.1	1.5	0.6	0.25	3.1	0.6
Block B	**alpha**	**c**	**V**	**alpha**	**C**	**V**
Original	1	10	1	0.25	5	1
Pipeline	1	12	0.7	0.25	6	0.7
Parallel	1	16	0.6	0.25	7.5	0.6
pipeline+clock gating	0.02	11	0.7	0.25	6.5	0.7
parallel+clock gating	0.05	18	0.6	0.25	8	0.6

(a) [5%] Please calculate power reduction with pipeline method. Power reduction = 100% - (power of pipeline/original power).

(b) [5%] Please calculate power reduction with parallel method. Power reduction = 100% - (power of parallel/original power)

(c) [6%] redo (a) and (b) for clock gating case, and comments that how these power reduction (pipeline vs. parallel, clock gating) techniques saves the power

(d) [6%] If only one result from Block A and Block B will be sent to the output, and Block A is much faster than Block B, please comment how you apply the data gating (or called operand isolation) and multi-Vt process to further reduce the power.

6. [12%] SoC Design Trend:

What is HIVE architecture? Please comment this new non-V**on Neumann** concept after reading the attached report from EE times.